IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A memory device, comprising:

a buffer memory having a plurality of addressable memory registers; the buffer memory capable of being partitioned into a plurality of buffer regions;

a counter having a plurality of storage registers, each storage register being associated with a respective buffer region of the buffer memory;

a logic network for writing and reading data into and out of ~~said~~ the buffer memory, ~~said~~ the logic network for partitioning ~~said~~ the buffer memory into [[a]] the plurality of buffer regions, wherein ~~said~~ the logic network writes/reads ~~and reads~~ data from a plurality of unique data classes into/from ~~said~~ the plurality of buffer regions such that each data class is uniquely written into and uniquely read from a different buffer region, and wherein ~~said~~ the logic network increments a value in a respective storage register associated with a respective buffer region each time that buffer region reaches a predetermined usage level; and

a timer for periodically sending a timing signal to ~~said~~ the logic network, the period of the timing signal defining a timing window;

wherein in response to ~~said~~ the timing signal, ~~said~~ the logic network:

recalls ~~data~~ the respective values from ~~said~~ the ~~counter~~ storage registers; whereby the respective value stored in each storage register indicates a number of times that the respective buffer region reaches the predetermined usage level within the timing window; and

re-partitions ~~said~~ the buffer memory according to the respective value having a highest value such that a more utilized buffer region is assigned more of the addressable memory registers.

2. (Currently Amended) A memory device according to claim 1 wherein ~~said~~ the logic network assigns a buffer region that is used less often fewer addressable memory registers.

3. (Original) A memory device according to claim 1 wherein each buffer region is always assigned at least a minimum number of addressable memory registers.

4. (Currently Amended) A memory device according to claim 1 wherein ~~said~~ the predetermined usage level is full.

5. (Previously Presented) A memory device according to claim 1 wherein when a least used buffer region is assigned a minimum number of addressable memory registers the logic network assigns a buffer region that is less often fully utilized but that has more than the minimum number of addressable memory registers.

6. (Currently Amended) A memory device according to claim 1 wherein ~~said~~ the data classes represent virtual lanes.

7. (Currently Amended) A memory device according to claim 1 wherein ~~said~~ the timing signal initiates clearing of ~~said~~ the plurality of storage registers.

8. (Currently Amended) A switch network comprising:

a network switch;

a card adaptor for transmitting and receiving data from ~~said~~ the network switch, and

a memory device for storing data for and from ~~said~~ the card adaptor, ~~said~~ the memory having:

a buffer memory having a plurality of addressable memory registers; the buffer memory capable of being partitioned into a plurality of buffer regions;

a counter having a plurality of storage registers, each storage register being associated with a respective buffer region of the buffer memory;

a logic network for writing and reading data into and out of ~~said~~ the buffer memory, ~~said~~ the logic network for partitioning ~~said~~ the buffer memory into [[a]] the plurality of buffer regions, wherein ~~said~~ the logic network writes/reads ~~and reads~~ data from a plurality of unique data classes into/from ~~said~~ the plurality of buffer regions such that each data class is uniquely written into and uniquely

read from a different buffer region, and wherein ~~said~~ the logic network increments a value in a respective storage register associated with a respective buffer region each time that buffer region reaches a predetermined usage level; and

a timer for periodically sending a timing signal to ~~said~~ the logic network, the period of the timing signal defining a timing window;

wherein in response to ~~said~~ the timing signal ~~said~~ the logic network:

recalls ~~data~~ the respective values from ~~said~~ the ~~counter~~ storage registers, whereby the respective value stored in each storage register indicates a number of times that the respective buffer region reaches the predetermined usage level within the timing window; and

re-partitions ~~said~~ the buffer memory according to the respective value having a highest value such that a more utilized buffer region is assigned more of the addressable memory registers.

9. (Currently Amended) A switch network according to claim 8 wherein ~~said~~ the logic network assigns a buffer region that is used less often fewer addressable memory registers.

10. (Original) A switch network according to claim 8 wherein each buffer region is always assigned at least a minimum number of addressable memory registers.

11. (Currently Amended) A switch network according to claim 8 wherein ~~said~~ the predetermined usage level is full.

12. (Previously Presented) A switch network according to claim 8 wherein when a least used buffer region is assigned a minimum number of addressable memory registers the logic network assigns a buffer region that is less often fully utilized but that has more than the minimum number of addressable memory registers.

13. (Currently Amended) A switch network according to claim 8 wherein ~~said~~ the data classes represent virtual lanes.

14. (Currently Amended) A switch network according to claim 8 wherein ~~said~~ the timing signal initiates clearing of ~~said~~ the plurality of storage registers.

15. (Currently Amended) A switch network according to claim 8 wherein ~~said~~ the card adaptor is a host channel adaptor.

16. (Currently Amended) A switch network according to claim 15 wherein ~~said~~ the host channel adaptor is an Infiniband host channel adaptor.

17. (Currently Amended) A switch network according to claim 8 wherein ~~said~~ the card adaptor is a target channel adaptor.

18. (Currently Amended) A switch network according to claim 17 wherein ~~said~~ the host channel adaptor is an Infiniband host channel adaptor.

19. (Currently Amended) A switch network according to claim 8 further including a central processing unit for sending data to and receiving data from ~~said~~ the memory device.

20. - 22. (Cancelled)

Please add the following new claim:

23. (New) A memory device, comprising:

a buffer memory having a plurality of addressable memory registers; the buffer memory capable of being partitioned into a plurality of buffer regions;

a counter having a plurality of storage registers, each storage register being associated with a respective buffer region of the buffer memory;

a logic network for writing and reading data into and out of the buffer memory, ~~said~~ the logic network for partitioning the buffer memory into the plurality of buffer regions, wherein the logic network increments a value in a respective storage register

associated with a respective buffer region each time that buffer region reaches a predetermined usage level; and

a timer for periodically sending a timing signal to the logic network, the period of the timing signal defining a timing window;

wherein in response to the timing signal, the logic network:

retrieves the respective values from the storage registers; whereby the respective value stored in each storage register indicates a number of times that the respective buffer region reaches the predetermined usage level within the timing window; and

re-partitions the buffer memory according to the respective value.